Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.070”**

**PAD FUNCTION:**

1. **IN1**
2. **D1**
3. **S1**
4. **VSS**
5. **GND**
6. **S4**
7. **D4**
8. **IN4**
9. **IN3**
10. **D3**
11. **S3**
12. **VL**
13. **VDD**
14. **S2**
15. **D2**
16. **IN2**

**3 2 1 16 15 14**

**4**

**5**

**13**

**12**

**6 7 8 9 10 11**

**MASK**

**REF**

**.093”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .003” x .003”**

**Backside Potential: VDD**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .070” X .093” DATE: 6/20/22**

**MFG: ANALOG DEVICES THICKNESS .015” P/N: ADG433B**

**DG 10.1.2**

#### Rev B, 7/19/02